IN THE CLAIMS:

Please cancel claims 7 - 17.

consumption in an reducing power 1. method of integrated circuit communication link having a logic logic circuitry including supplycircuitry, the voltage-critical logic circuitry and non-supplymethod logic circuitry, the voltage-critical comprising the steps of:

synthesizing the integrated circuit to identify the supply-voltage-critical logic circuitry;

isolating the supply-voltage-critical logic circuitry from the non-supply-voltage-critical logic circuitry, the supply-voltage-critical logic circuitry being driven by a first supply voltage and the non-supply-voltage-critical logic circuitry being driven by a second supply voltage, the first supply voltage being greater than the second supply voltage;

embedding a voltage regulator in the communication link for supplying the second voltage; and

selectively interfacing the supply-voltage-critical logic circuitry with the non-supply-voltage-critical logic circuitry using level shifters.

2. The method of Claim 1 wherein the first voltage is supplied to the communication link.

- 3. The method of Claim 2 wherein the first voltage is used to generate the second voltage.
- 4. The method of Claim 3 wherein the selectively interfacing step includes the step of selecting a minimal number of points at which the supply-voltage-critical logic circuitry interfaces with the non-supply-voltage-critical logic circuitry.
- 5. The method of Claim 4 wherein a level shifter is used at each interfacing point.
- 6. The method of Claim 5 wherein the communication link is on a chip, the chip having a multiplicity of communication links, a plurality of the multiplicity of the communication links sharing the embedded voltage regulator.

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reducing power consumption in 18. method of integrated circuit communication link having logic logic circuitry including circuitry, the logic circuitry and non-supplyvoltage-critical the method circuitry, logic voltage-critical comprising the steps of:

determining and isolating the supply-voltage-critical logic circuitry from the non-supply-voltage-critical logic circuitry, the supply-voltage-critical logic circuitry being driven by a first supply voltage and the non-supply-voltage-critical logic circuitry being

driven by a second supply voltage, the first supply voltage being greater than the second supply voltage;

embedding a voltage regulator in the communication link for supplying the second voltage: and

selectively interfacing the supply-voltage-critical logic circuitry with the non-supply-voltage-critical logic circuitry using level shifters.

- 19. The method of Claim 18 wherein the determining step includes the step of synthesizing the communication link using the second voltage to identify the supply-voltage-critical logic circuitry.
- 20. The method of Claim 19 wherein the communication link is on a chip, the chip having a multiplicity of communication links, a plurality of the multiplicity of the communication links sharing the embedded voltage regulator.